FPGA Project

D-PHY Testbench

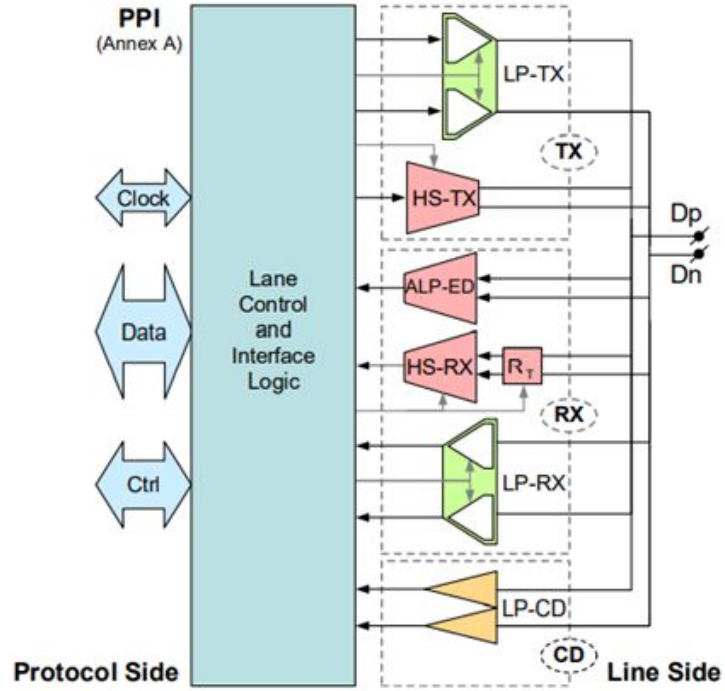
(TX ⇔ RX)

twwang97

January 11, 2026

Introduction

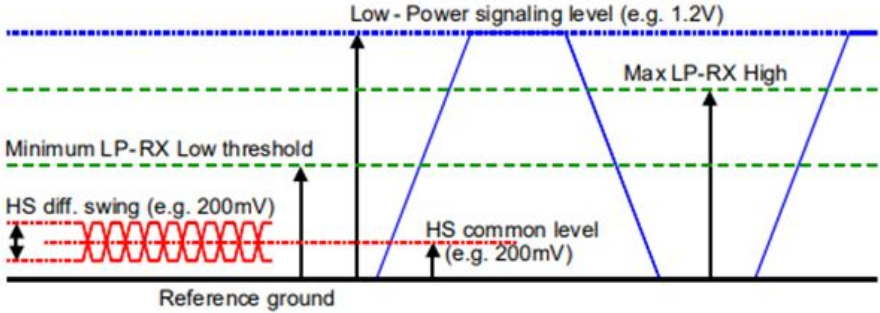
- D-PHY lanes switch between Low-Power (**LP**, single-ended) and High-Speed (**HS**, differential) electrical levels and states.
- D-PHY lanes are operated in three modes — **Control** (LP idle/stop), High-Speed **bursts** (data), and **Escape** (ultra-low-power commands).
- Lane states: E.g., LP-11 stop/idle, LP-00, LP-01/10, HS-0, HS-1). Lane levels refer to the electrical signaling: low-power single-ended levels (DP or DN pulled high/low relative to ground) and high-speed differential levels (DP/DN differential pair toggling). A lane is physically in Control (LP) when idle and on enters HS during bursts of high-speed differential signaling.



Lane state descriptions

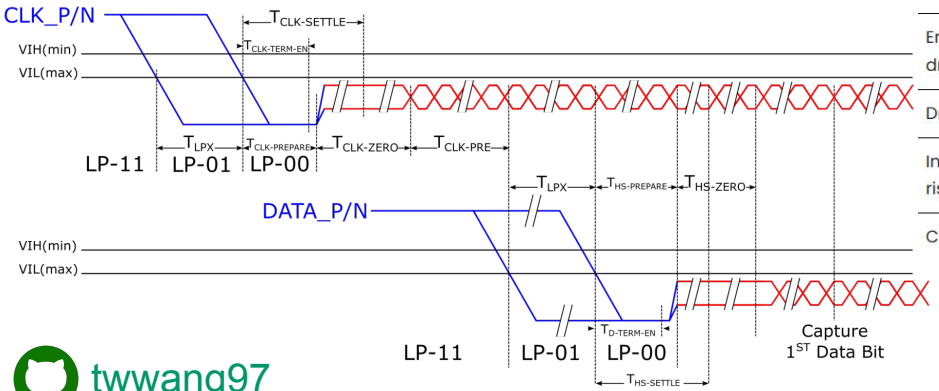
State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A[1]	N/A[2]
HS-1	HS High	HS Low	Differential-1	N/A[3]	N/A[4]
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Request	Mark-0
LP-10	LP High	LP Low	N/A	LP-Request	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A[5]

[1] During High-Speed transmission, the Low-Power receivers observe LP-00 on the Lines.
[2] During High-Speed transmission, the Low-Power receivers observe LP-00 on the Lines.
[3] During High-Speed transmission, the Low-Power receivers observe LP-00 on the Lines.
[4] During High-Speed transmission, the Low-Power receivers observe LP-00 on the Lines.
[5] If LP-11 occurs during Escape mode, the Lane returns to Stop state (Control Mode LP-11).



start of transmission (SoT)

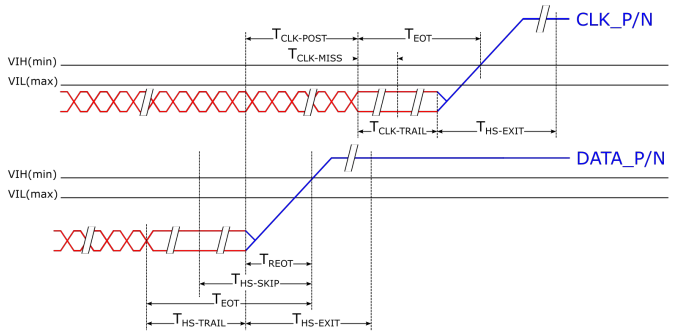
- The transition from a stop state (**LP-11**) into high-speed (**HS**) data transmission mode takes two steps. The clock lane (**cl**) enters HS clock mode before the data lane (**dl**) enters HS mode.



TX side	RX side
Drives Stop state (LP-11)	Observes Stop state
Drives HS-Req state (LP-01) for time TLPX	Observes transition from LP-11 to LP-01 on the Lines
Drives Bridge state (LP-00) for time T_{CLK}-PREPARE	Observes transition from LP-01 to LP-00 on the Lines. Enables Line Termination after time TCLK-TERM-EN
Enables High-Speed driver and disables Low-Power drivers simultaneously.	Enables HS-RX and waits for timer $T_{CLK-SETTLE}$ to expire in order to neglect transition effects.
Drives HS-0 for a time $T_{CLK-ZERO}$	Receives HS-signal
Drives the High-Speed Clock signal for time period TCLK-PRE before any Data Lane starts up	Receives High-Speed Clock signal

TX side	RX side
Drives Stop state (LP-11)	Observes Stop state
Drives HS-Req state (LP-01) for time TLPX	Observes transition from LP-11 to LP-01 on the Lines
Drives Bridge state (LP-00) for time THS-PREPARE	Observes transition from LP-01 to LP-00 on the Lines, enables Line Termination after time TD-TERM-EN
Enables High-Speed driver and disables Low-Power drivers simultaneously.	Enables HS-RX and waits for timer THS-SETTLE to expire in order to neglect transition effects
Drives HS-0 for a time THS-ZERO	Starts looking for Leader-Sequence
Inserts the HS Sync-Sequence '00011101' beginning on a rising Clock edge	Synchronizes upon recognition of Leader Sequence `011101`
Continues to Transmit High-Speed payload data	Receives payload data

end of transmission (EoT)



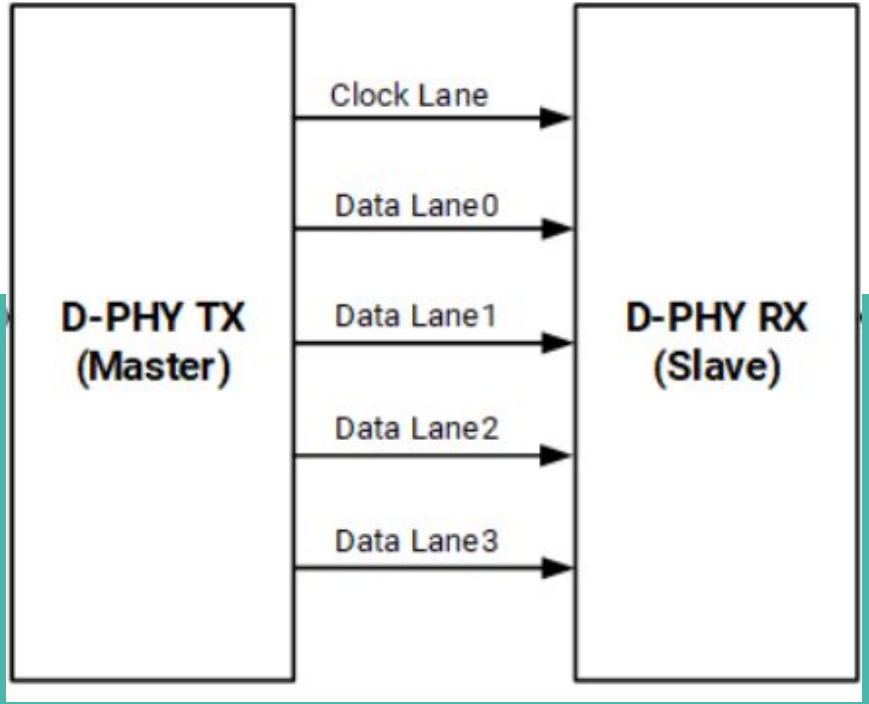
- At the end of a High-Speed Data burst, a data lane leaves High-Speed (**HS**) transmission mode and enters the **stop state** with an End-of-Transmission (**EoT**) procedure.

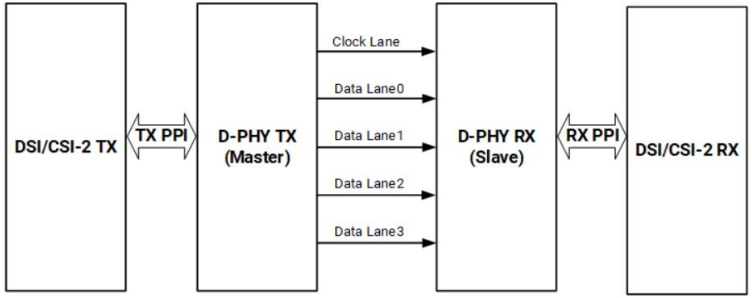
TX side	RX side
Completes transmission of payload data	Receives payload data
Toggles differential state immediately after last payload data bit and keeps that state for a time THS-TRAIL	
Disables the HS-TX, enables the LP-TX, and drives Stop state (LP-11) for a time THS-EXIT	Detects the Lines leaving LP-00 state and entering Stop state (LP-11) and disables Termination
	Neglect bits of last period THS-SKIP to hide transition effects
	Detect last transition in valid Data, determine last valid data byte, and skip trailer sequence

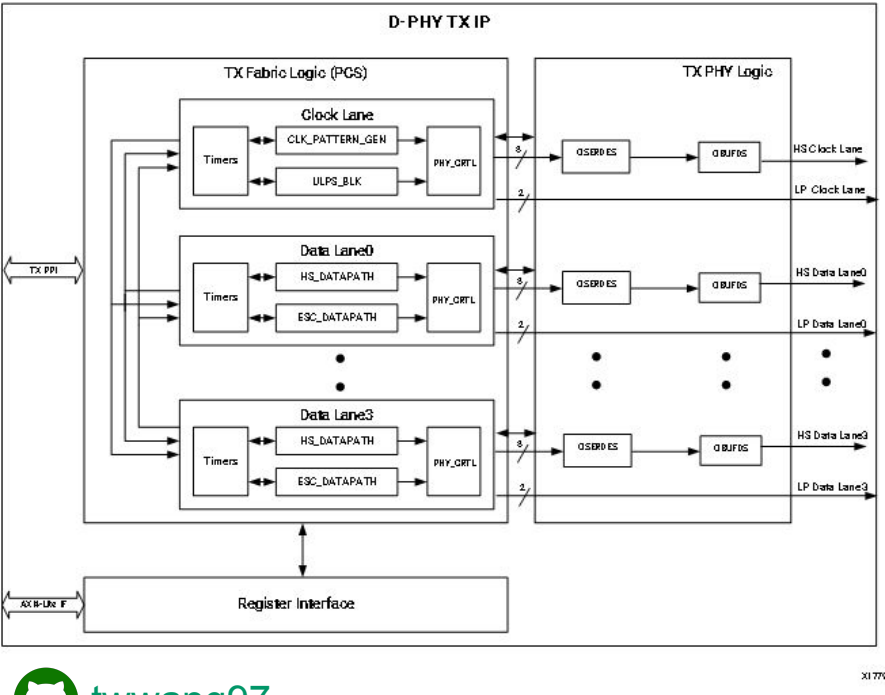
continuous clock mode

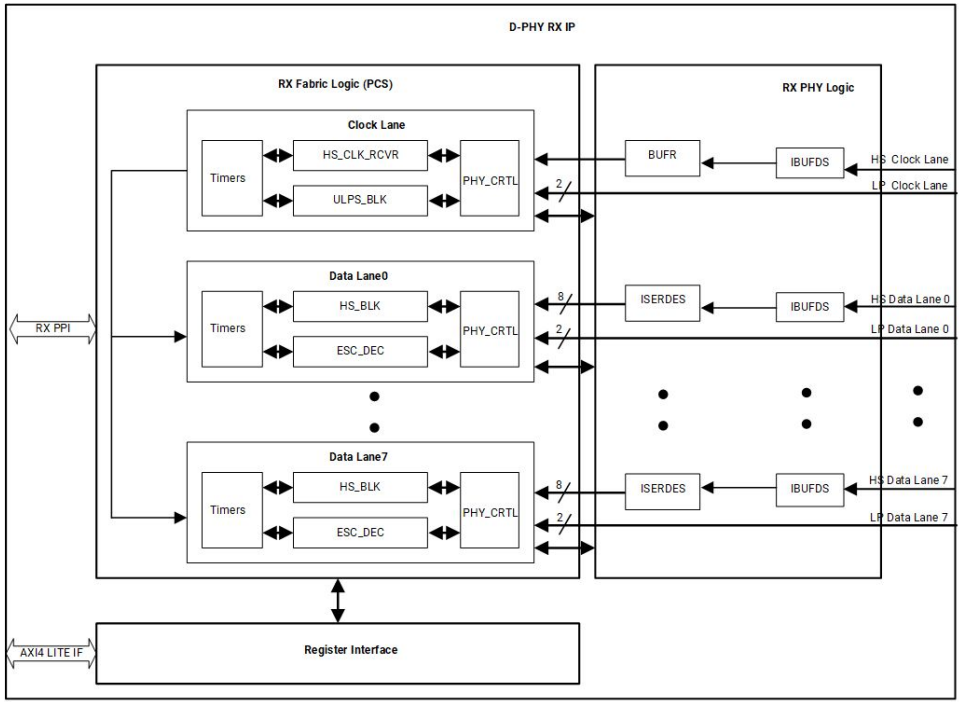
- Both the CSI-2 and DSI specifications support a continuous clock mode.
- For **continuous** clock behavior, the Clock Lane (CL) remains in high-speed mode generating active clock signals between HS data packet transmissions.
- For **non-continuous** clock behavior, the CL enters the **LP-11** state between HS data packet transmissions.
- Continuous clock mode allows for higher data rates, because the timing overhead of exiting and reentering HS-mode on the clock lane is eliminated.

D-PHY Testbench in XSim



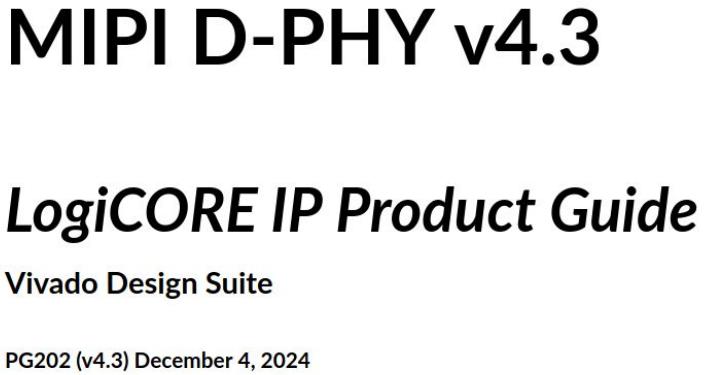

DSI/CSI-2 TX
TX PPI
D-PHY TX (Master)
Clock Lane
Data Lane0
Data Lane1
Data Lane2
Data Lane3
D-PHY RX (Slave)
RX PPI
DSI/CSI-2 RX


D-PHY TX IP
TX Fabric Logic (PCS)
TX PHY Logic
Clock Lane
Timers
CLK_PATTERN_GEN
ULPS_BLK
PHY_CRTL
OSERDES
OBUFDS
HS Clock Lane
LP Clock Lane
Data Lane0
HS_DATAPATH
ESC_DATAPATH
HS Data Lane0
LP Data Lane0
Data Lane3
HS Data Lane3
LP Data Lane3
TX PPI
AXI4-Lite IF
Register Interface


D-PHY RX IP
RX Fabric Logic (PCS)
RX PHY Logic
Clock Lane
Timers
HS_CLK_RCVR
ULPS_BLK
PHY_CRTL
BUFR
IBUFDS
HS Clock Lane
LP Clock Lane
Data Lane0
HS_BLK
ESC_DEC
ISERDES
HS Data Lane 0
LP Data Lane 0
RX PPI
Data Lane7
HS Data Lane 7
LP Data Lane 7
AXI4 LITE IF
Register Interface

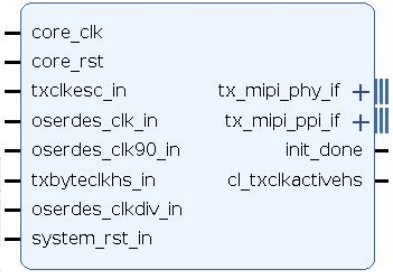
Platform

- Library: Xilinx **MIPI TX** and **MIPI RX** detailed in the official PG202 document.
- Vivado Version: 2025.2.
- Testbench Language: Verilog-2001.
- Simulation: XSim (Vivado Simulator).



AMD
Vivado 2025.2

D-PHY v4.3



Component Name: xilinx_dphy_tx_v4_3

Core Configuration | Shared Logic

Core Parameters

- D-PHY Lanes: 4
- Line Rate (Mbps): 1500
- [x] Linerate supported by Device Datasheet
- Data Flow: TX
- Esc Clk (MHz): 20.000
- LPX Period (ns): 50
- Resource optimization presets: None

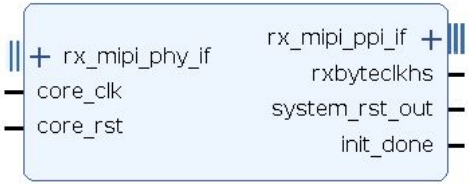
Control and Debug

- [ ] Enable Active lanes support
- [ ] Infer OBUFTDS for 7-Series HS outputs
- [ ] Enable AXI-4 Lite Register I/F

Protocol Watchdog Timers

- [x] Enable HS and ESC Timeout Counters/Registers
- HS Timeout (Bytes): 65541
- Escape Timeout (ns): 25600

D-PHY Tx



Component Name: xilinx_dphy_rx_v4_3

- D-PHY Lanes: 4
- Line Rate (Mbps): 1500
- [x] Linerate supported by Device Datasheet
- Data Flow: RX
- Esc Clk (MHz): 20.000
- LPX Period (ns): 50
- [ ] D-PHY RX ULPS WAKEUP counter for 1 ms time
- Resource optimization presets: None

Control and Debug

- [ ] Enable AXI-4 Lite Register I/F

Protocol Watchdog Timers

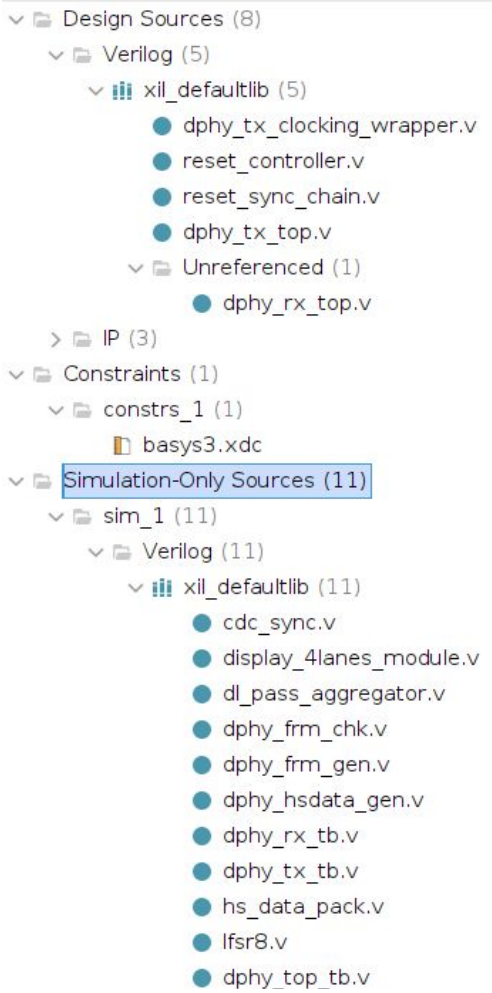
- [x] Enable HS and ESC Timeout Counters/Registers
- HS Timeout (Bytes): 65541
- Escape Timeout (ns): 25600

Calibration Mode

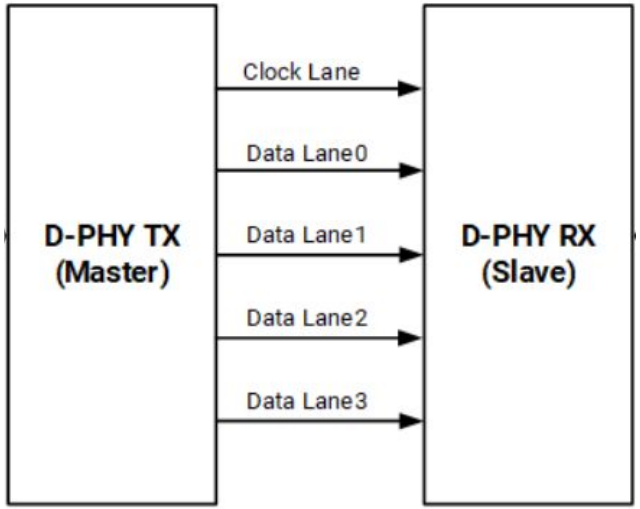
- (•) NONE ( ) FIXED ( ) AUTO

D-PHY Rx

Write Verilog (*.v) for simulation

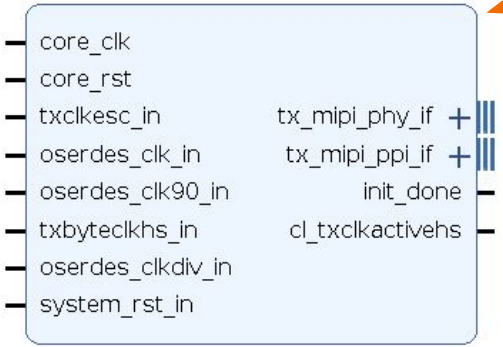


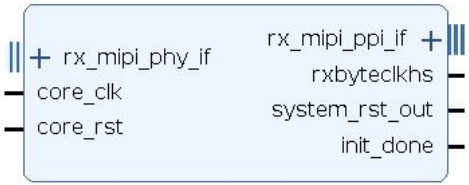
D-PHY Testbench in XSim

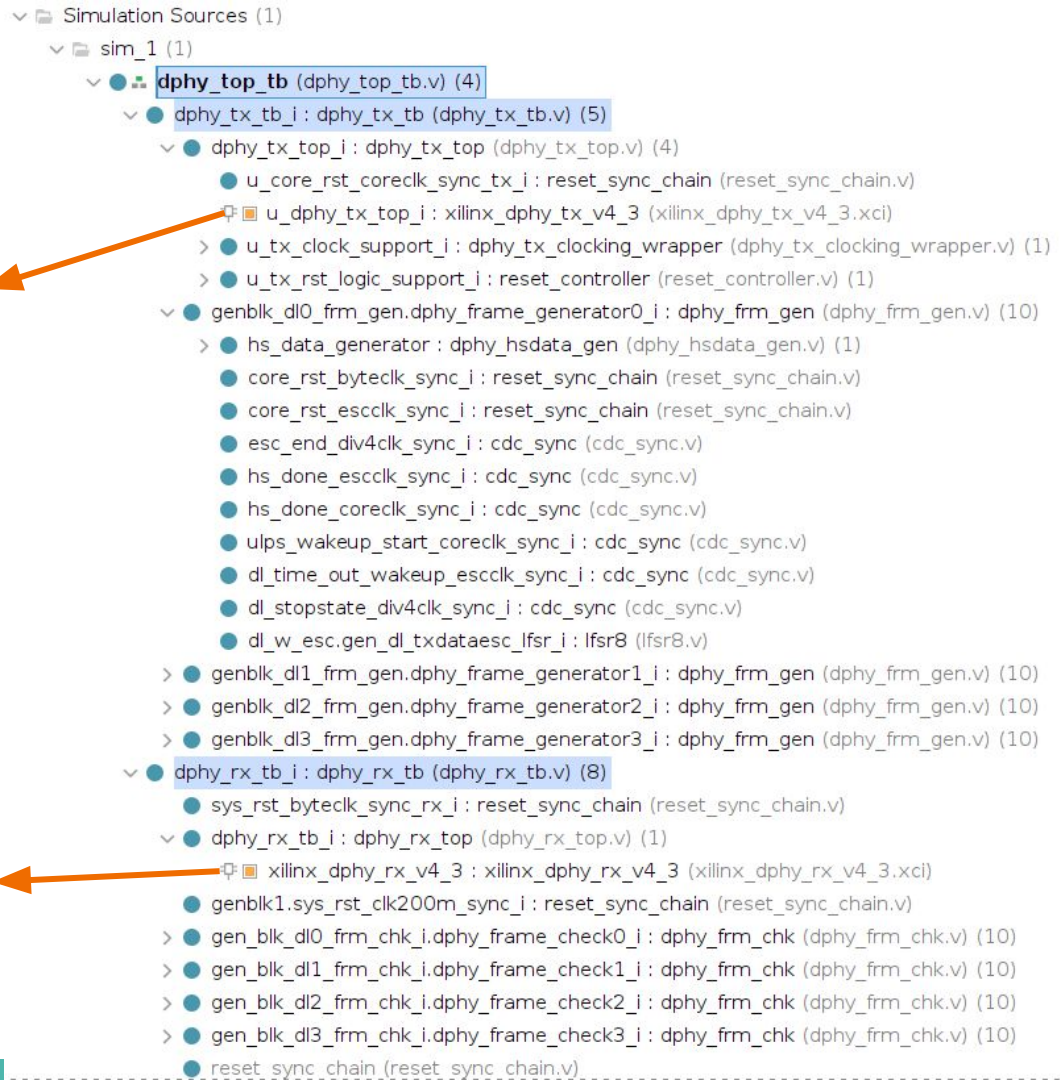


- Simulation Sources (1)
  - sim_1 (1)
    - **dphy_top_tb** (dphy_top_tb.v) (4)
      - dphy_tx_tb_i : dphy_tx_tb (dphy_tx_tb.v) (5)
        - dphy_tx_top_i : dphy_tx_top (dphy_tx_top.v) (4)
          - u_core_rst_coreclk_sync_tx_i : reset_sync_chain (reset_sync_chain.v)
          - u_dphy_tx_top_i : xilinx_dphy_tx_v4_3 (xilinx_dphy_tx_v4_3.xci)
          - u_tx_clock_support_i : dphy_tx_clocking_wrapper (dphy_tx_clocking_wrapper.v) (1)
          - u_tx_rst_logic_support_i : reset_controller (reset_controller.v) (1)
        - genblk_dl0_frm_gen.dphy_frame_generator0_i : dphy_frm_gen (dphy_frm_gen.v) (10)
          - hs_data_generator : dphy_hsdata_gen (dphy_hsdata_gen.v) (1)
          - core_rst_byteclk_sync_i : reset_sync_chain (reset_sync_chain.v)
          - core_rst_escclk_sync_i : reset_sync_chain (reset_sync_chain.v)
          - esc_end_div4clk_sync_i : cdc_sync (cdc_sync.v)
          - hs_done_escclk_sync_i : cdc_sync (cdc_sync.v)
          - hs_done_coreclk_sync_i : cdc_sync (cdc_sync.v)
          - ulps_wakeup_start_coreclk_sync_i : cdc_sync (cdc_sync.v)
          - dl_time_out_wakeup_escclk_sync_i : cdc_sync (cdc_sync.v)
          - dl_stopstate_div4clk_sync_i : cdc_sync (cdc_sync.v)
          - dl_w_esc.gen_dl_txdataesc_lfsr_i : lfsr8 (lfsr8.v)
        - genblk_dl1_frm_gen.dphy_frame_generator1_i : dphy_frm_gen (dphy_frm_gen.v) (10)
        - genblk_dl2_frm_gen.dphy_frame_generator2_i : dphy_frm_gen (dphy_frm_gen.v) (10)
        - genblk_dl3_frm_gen.dphy_frame_generator3_i : dphy_frm_gen (dphy_frm_gen.v) (10)
      - dphy_rx_tb_i : dphy_rx_tb (dphy_rx_tb.v) (8)
        - sys_rst_byteclk_sync_rx_i : reset_sync_chain (reset_sync_chain.v)
        - dphy_rx_tb_i : dphy_rx_top (dphy_rx_top.v) (1)
          - xilinx_dphy_rx_v4_3 : xilinx_dphy_rx_v4_3 (xilinx_dphy_rx_v4_3.xci)
        - genblk1.sys_rst_clk200m_sync_i : reset_sync_chain (reset_sync_chain.v)
        - gen_blk_dl0_frm_chk_i.dphy_frame_check0_i : dphy_frm_chk (dphy_frm_chk.v) (10)
        - gen_blk_dl1_frm_chk_i.dphy_frame_check1_i : dphy_frm_chk (dphy_frm_chk.v) (10)
        - gen_blk_dl2_frm_chk_i.dphy_frame_check2_i : dphy_frm_chk (dphy_frm_chk.v) (10)
        - gen_blk_dl3_frm_chk_i.dphy_frame_check3_i : dphy_frm_chk (dphy_frm_chk.v) (10)
        - reset_sync_chain (reset_sync_chain.v)

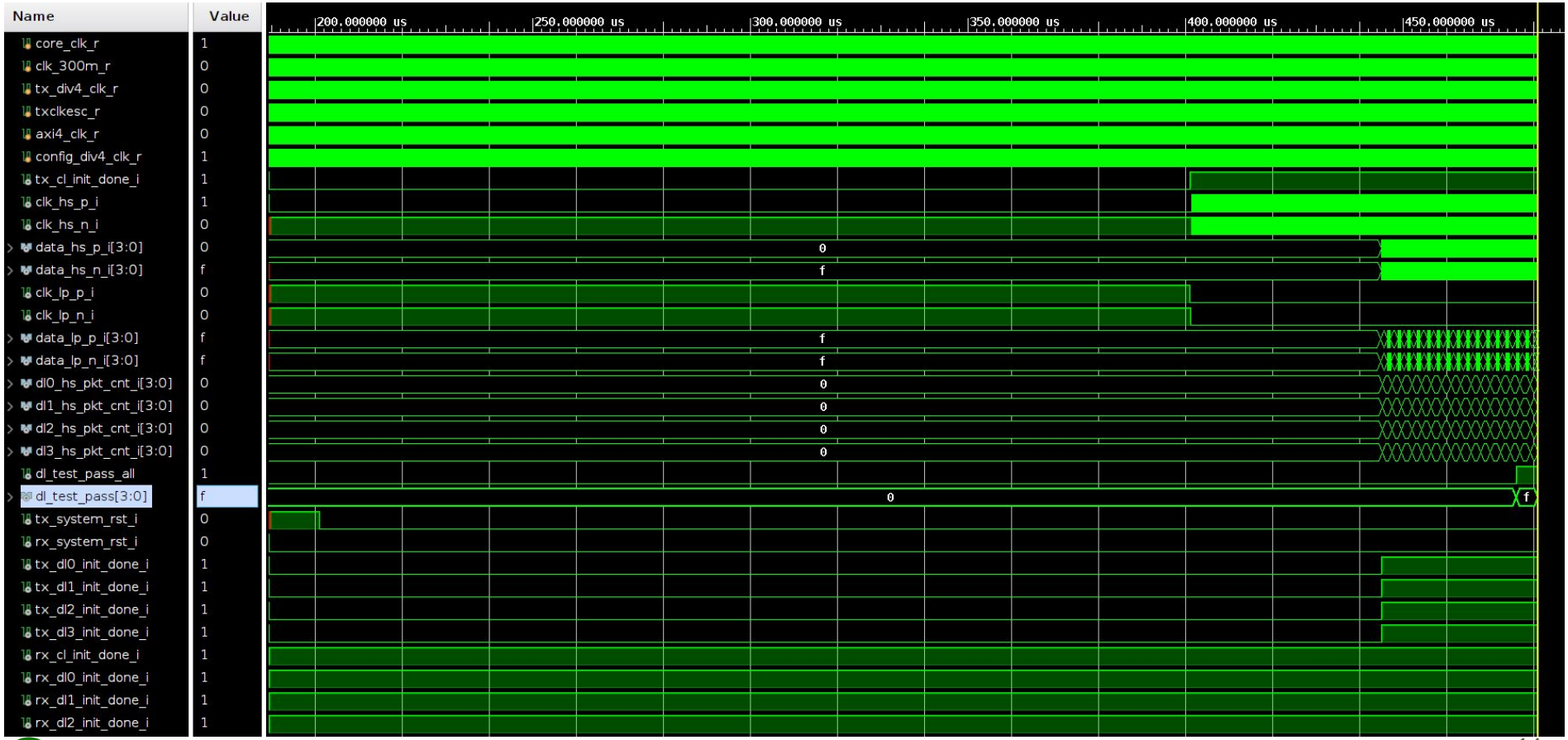
D-PHY Testbench in XSim



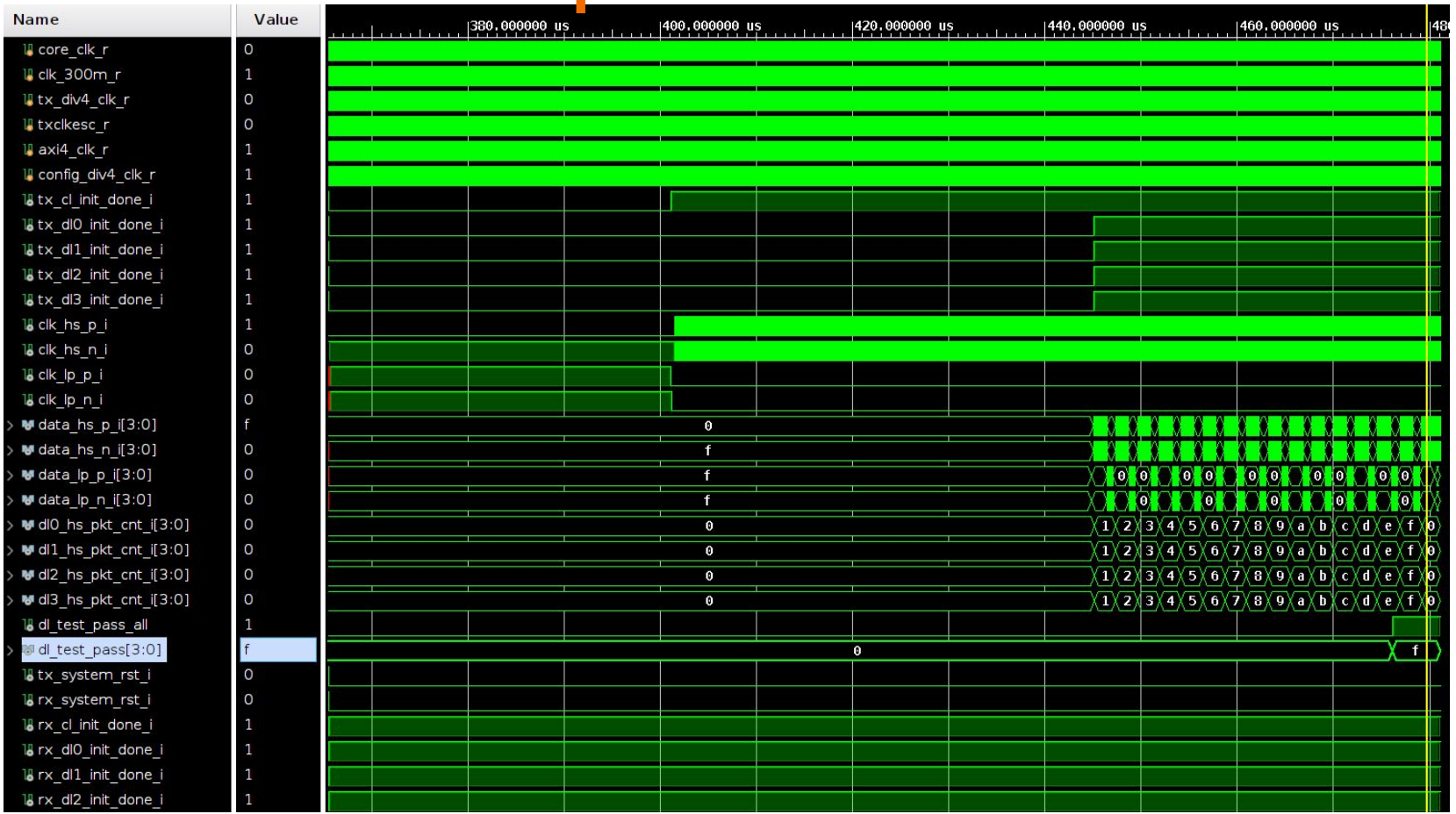




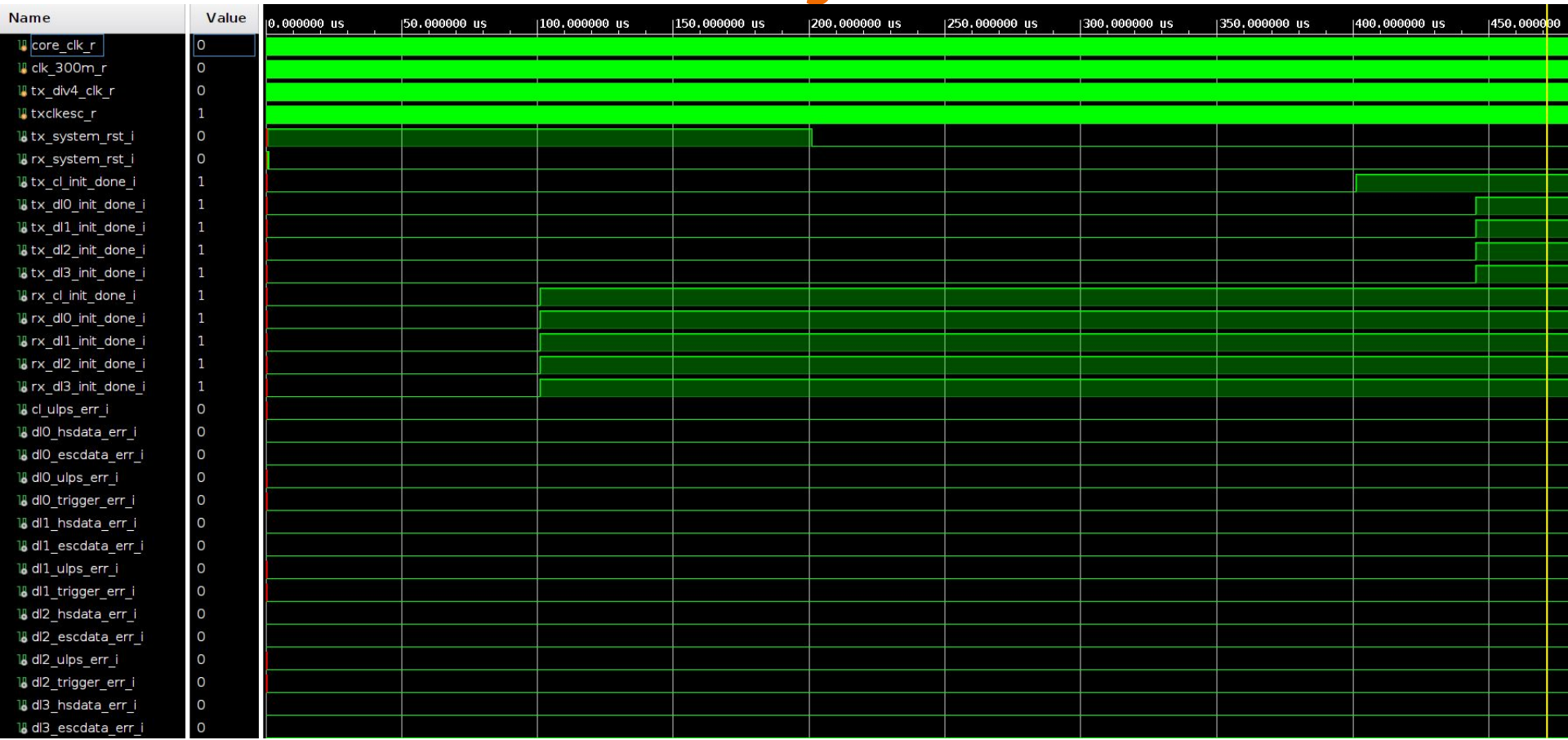
XSim Passed: ≥ 15 HS packets are collected!



XSim Passed: ≥ 15 HS packets are collected!

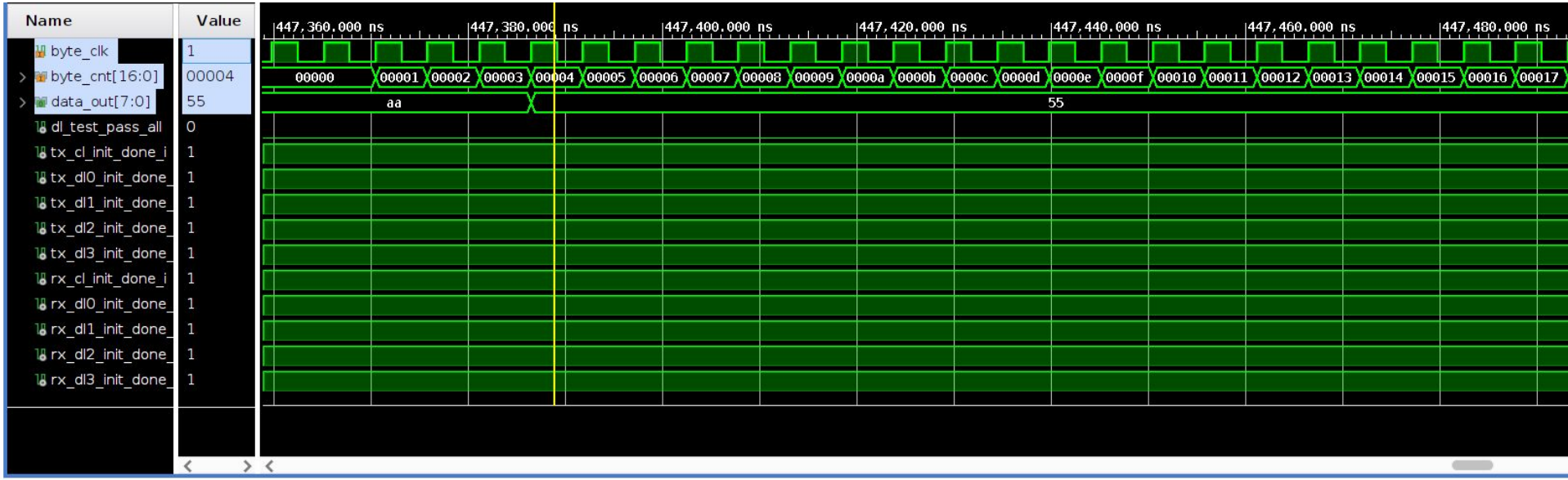


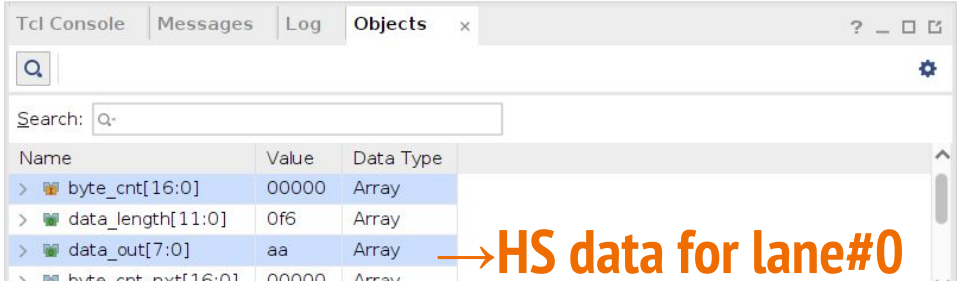
XSim Passed: NO error message!



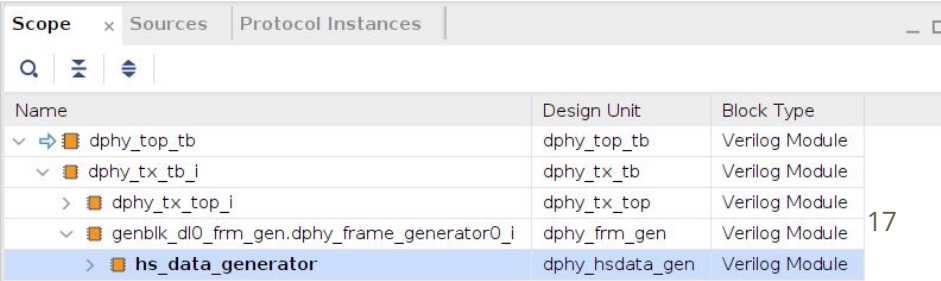
D-PHY Testbench in XSim

The test pattern for generated TX HS data is defined in dphy_hsdata_gen.v, and such a sequence is 0xAA S4, 0x55 S30, 0x33 S30, 0xF0 S30, 0x7F S30, 0x55 S30, 0x33 S30, 0xF0 S30, 0x80 S30, 0xAA S2.



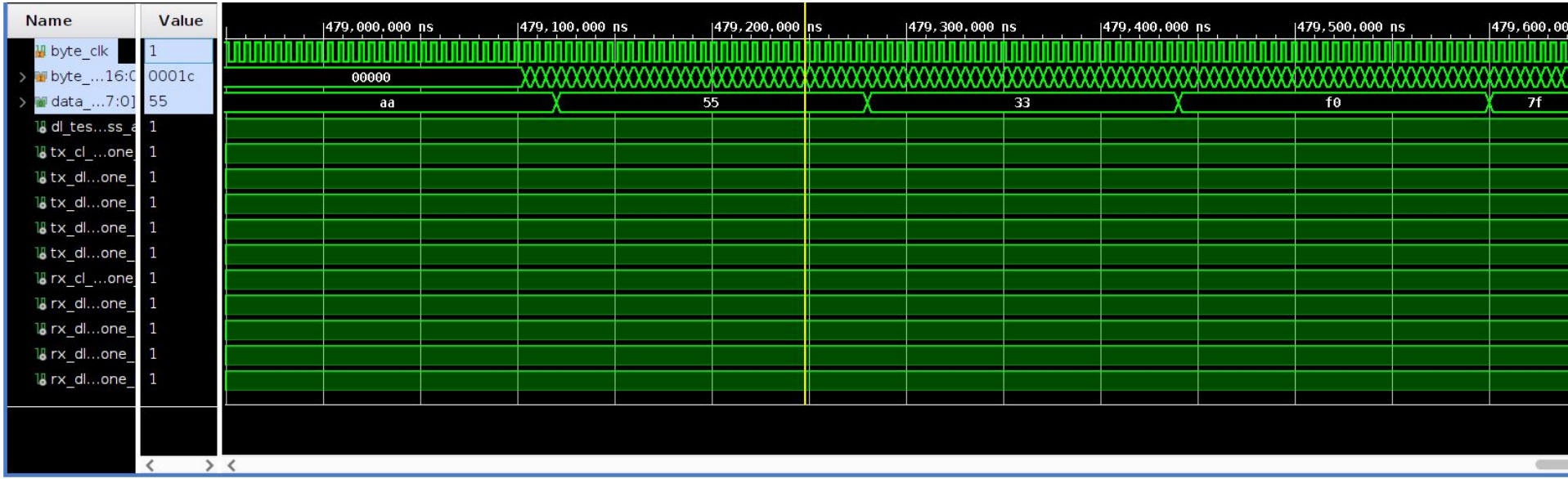


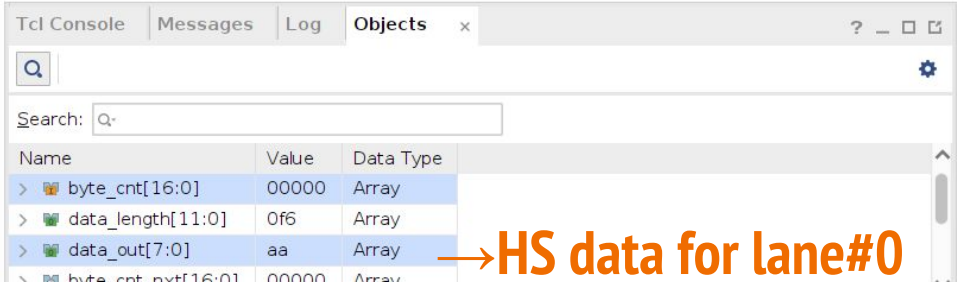
→HS data for lane#0



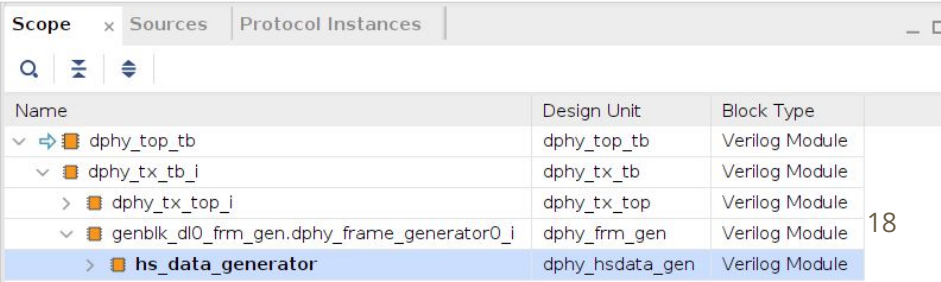
D-PHY Testbench in XSim

The test pattern for generated TX HS data is defined in dphy_hsdata_gen.v, and such a sequence is 0xAA S4, 0x55 S30, 0x33 S30, 0xF0 S30, 0x7F S30, 0x55 S30, 0x33 S30, 0xF0 S30, 0x80 S30, 0xAA S2.



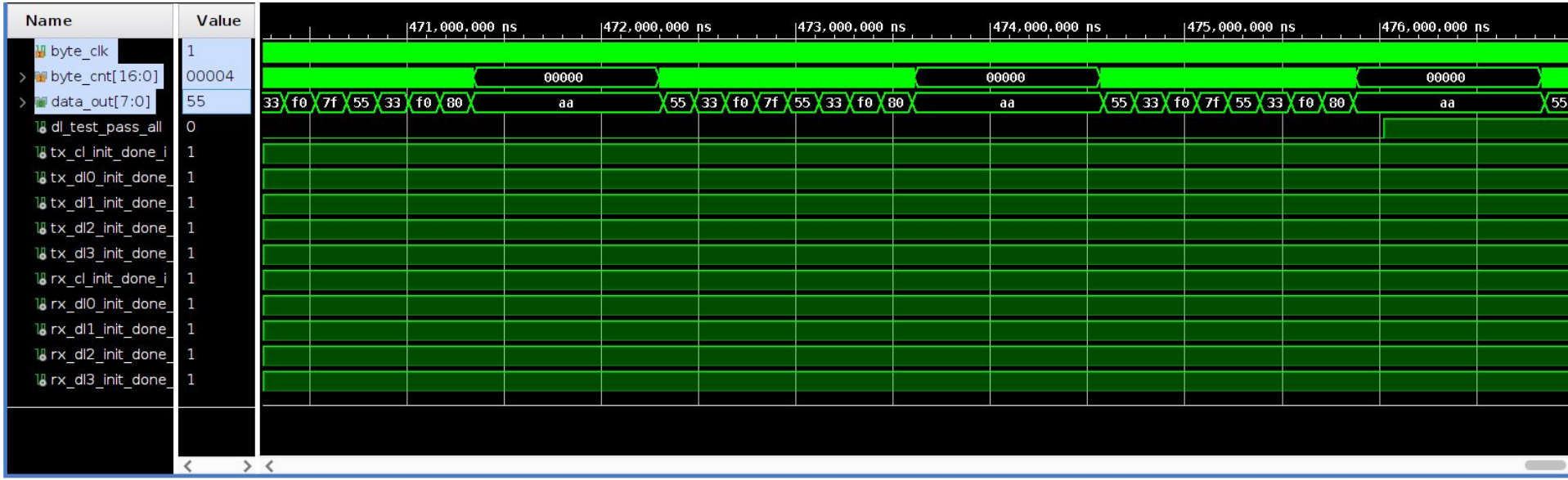


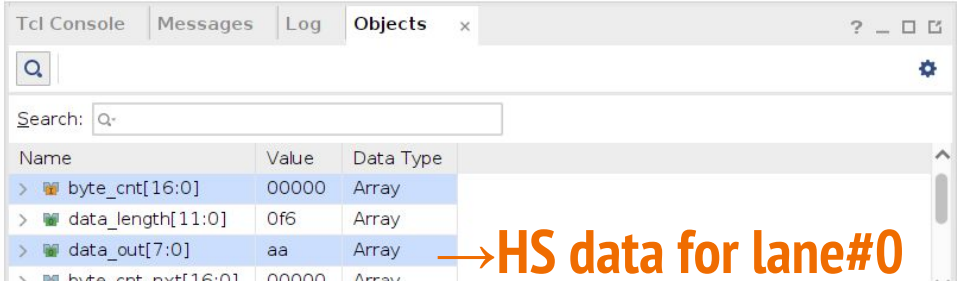
→HS data for lane#0



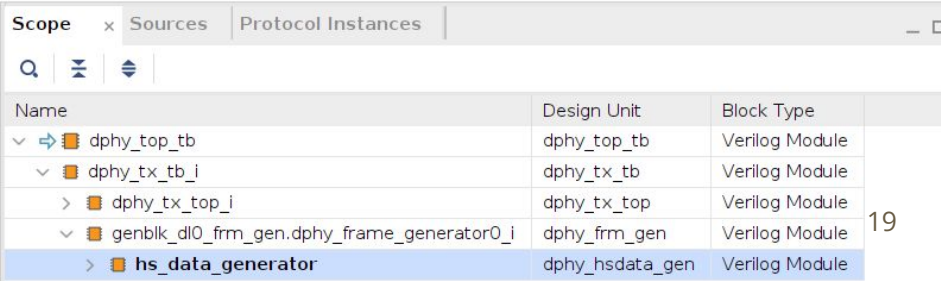
D-PHY Testbench in XSim

The test pattern for generated TX HS data is defined in dphy_hsdata_gen.v, and such a sequence is 0xAA S4, 0x55 S30, 0x33 S30, 0xF0 S30, 0x7F S30, 0x55 S30, 0x33 S30, 0xF0 S30, 0x80 S30, 0xAA S2.





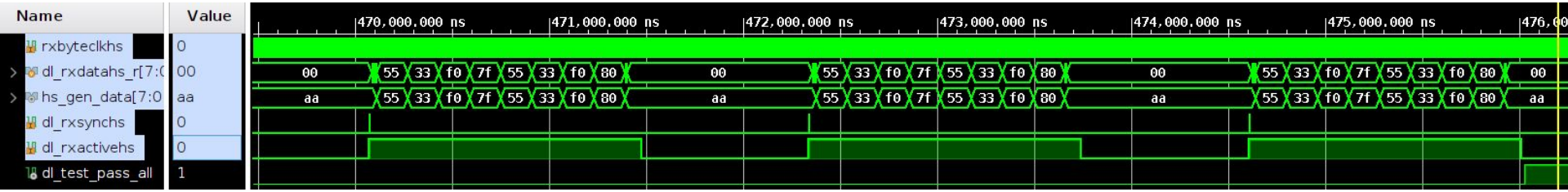
→HS data for lane#0

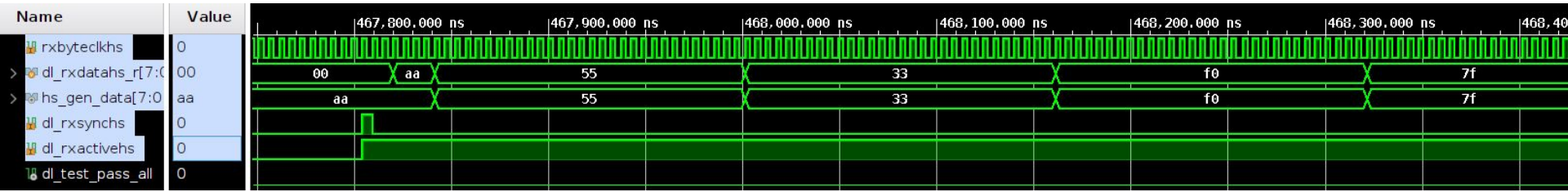


D-PHY Testbench in XSim

dphy_frm_chk.v

The data (dl_rxdatahs_r) received by D-PHY Rx should also be verified. The received dl_rxdatahs_r[7:0] (on data lane #0) triggered by the clock rxbyteclkhs is compared with the expected hs_gen_data[7:0].

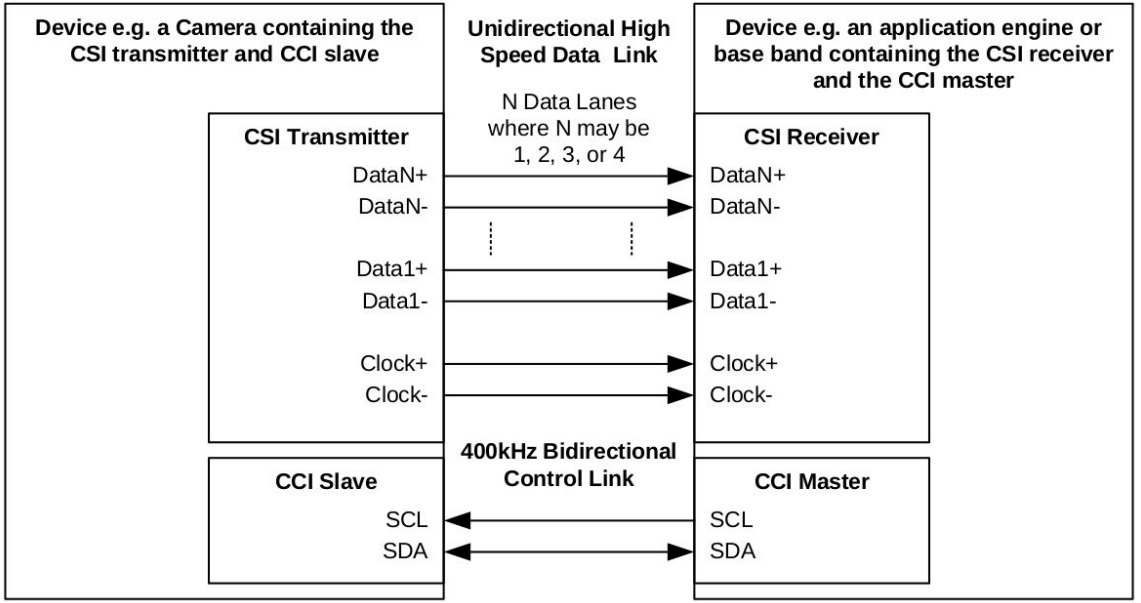




Application

GMSL camera → FPGA (MIPI) Connection

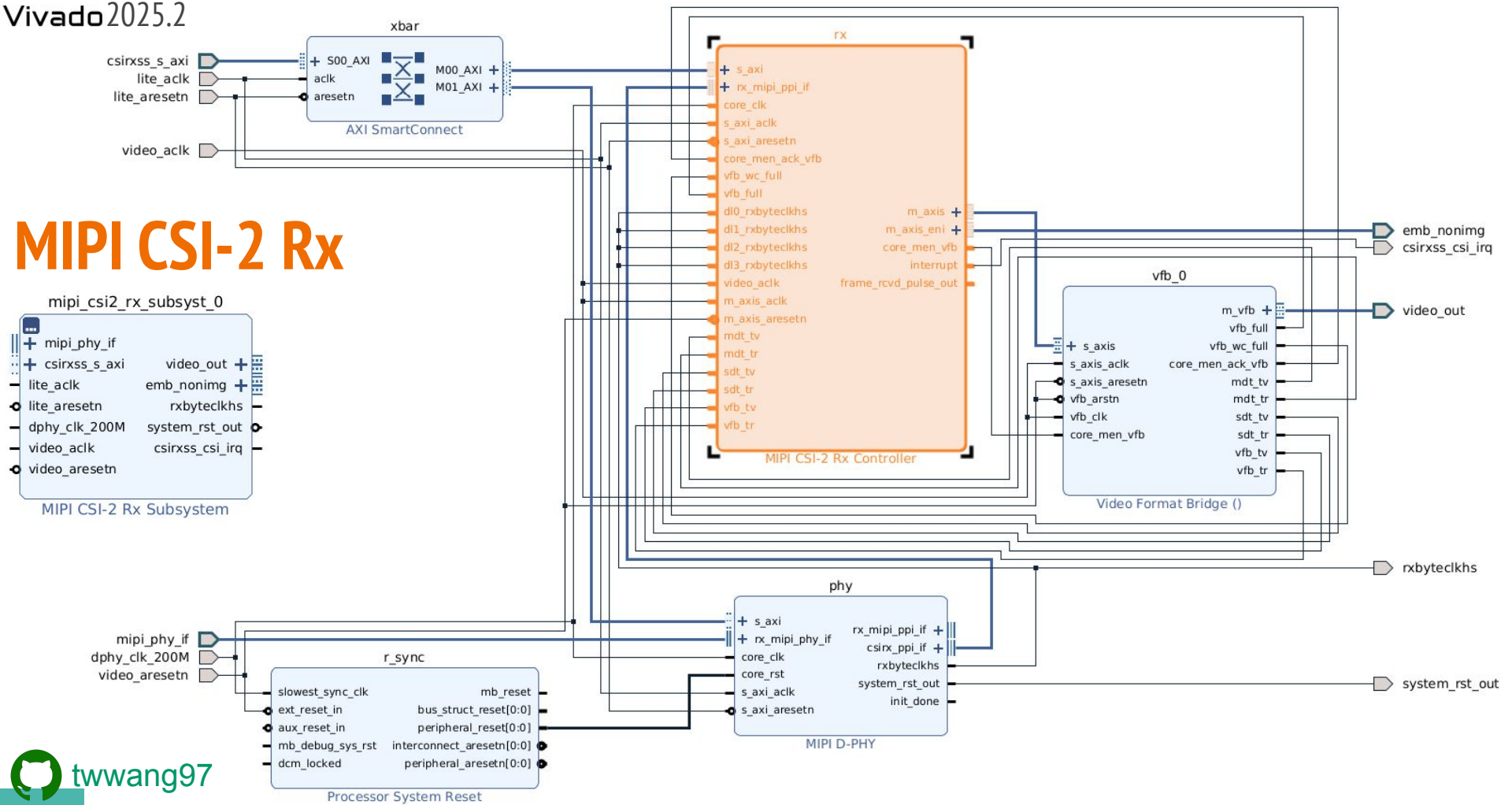
MIPI



- **MIPI** (Mobile Industry Processor Interface)
- **CSI** (Camera Serial Interface)
- **DSI** (Display Serial Interface)
- **CCI** (Camera Control Interface) is a subset of the I2C protocol.

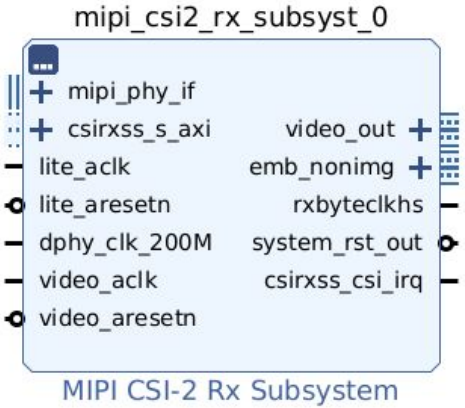
AMD
Vivado 2025.2

MIPI CSI-2 Rx



AMD
Vivado 2025.2

Document: PG232

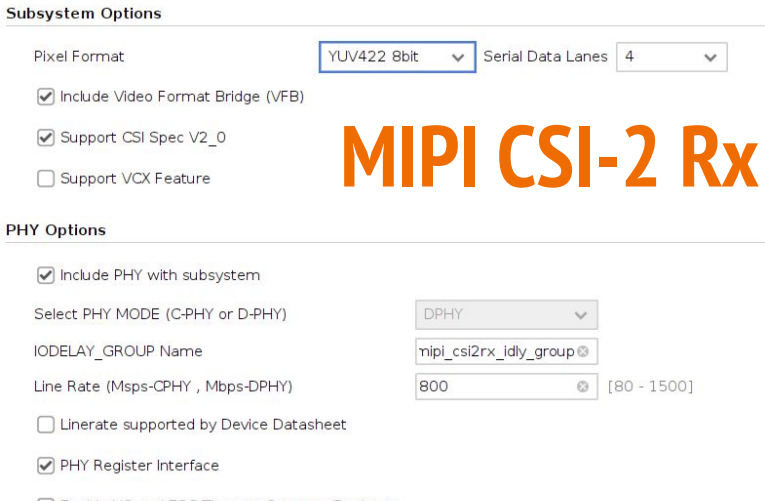


MIPI CSI-2 Receiver Subsystem v6.0

Product Guide

Vivado Design Suite

PG232 (v6.0) November 20, 2025



How to map a GMSL camera → FPGA (MIPI) connection?

- Camera side: A GMSL camera contains a **serializer** that packages sensor output into a GMSL SerDes stream and sends it over coax/**FAKRA**/UTP. Power and control (I^2C/MDIO) can be carried on the same cable in many implementations.
- Receiver side (near FPGA): The GMSL **deserializer** translates the long-reach **SerDes** into a standard **CSI-2** interface the FPGA can consume.

How to map a GMSL camera → FPGA (MIPI) connection?

Attribute	GMSL	MIPI CSI-2 (CSI2-Rx)
Purpose	Long-reach serialized camera link; cable/automotive use	Chip-to-chip camera interface (PHY + packet protocol)
Physical medium	Coax/UTP/flex; supports power over cable	Short PCB traces or flex; D-PHY/C-PHY lanes
Distance	Meters to tens of meters (automotive)	Millimeters to centimeters
Topology	Serializer/Deserializer (SerDes) pair; often with ARQ/robust features	Host receiver IP expecting CSI-2 packets
Error handling	Link-level robustness, sometimes ARQ/CRC	Packet framing, virtual channels, but not long-cable ARQ
Typical use	Cameras in vehicles, robotics where distance and EMI matter	Direct sensor → SoC/FPGA connections on board

References

- https://docs.nxp.com/bundle/AN13573/page/topics/dsi_examples.html
- https://www.cnblogs.com/fuzidage/p/14107768.html
- https://docs.amd.com/r/en-US/pg202-mipi-dphy