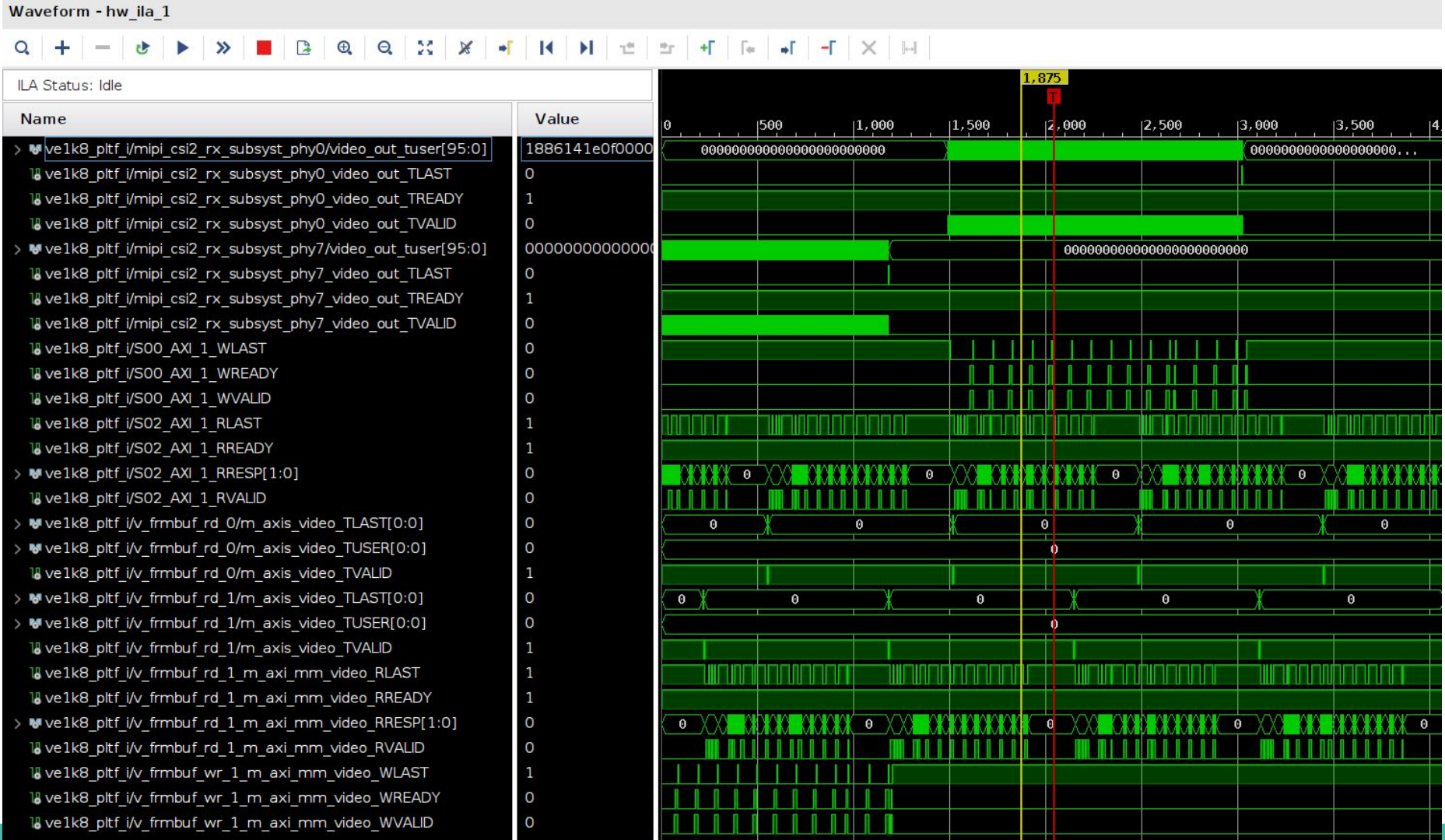
VE-1008

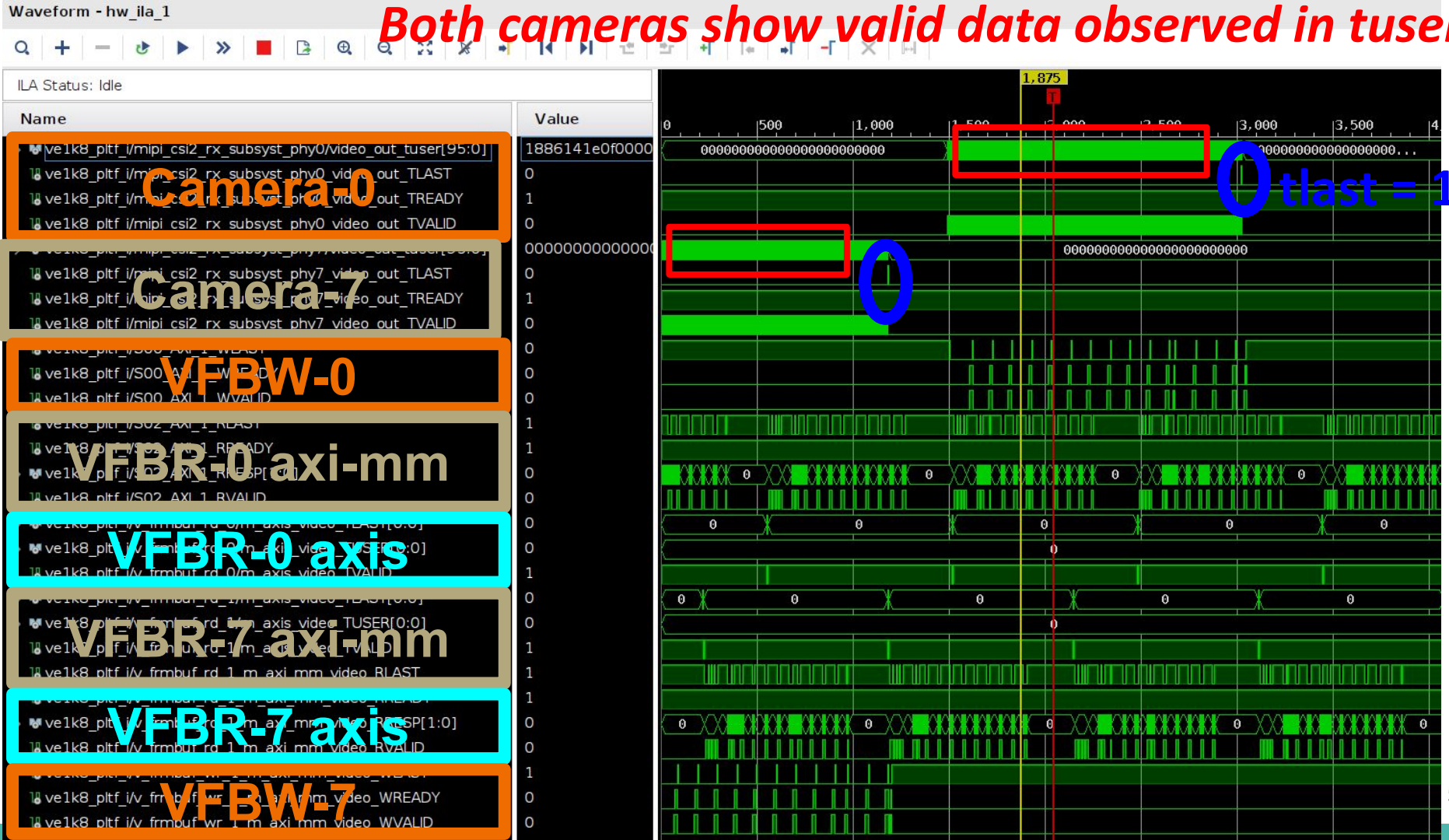
2 Cameras > BRAM > XDMA

David

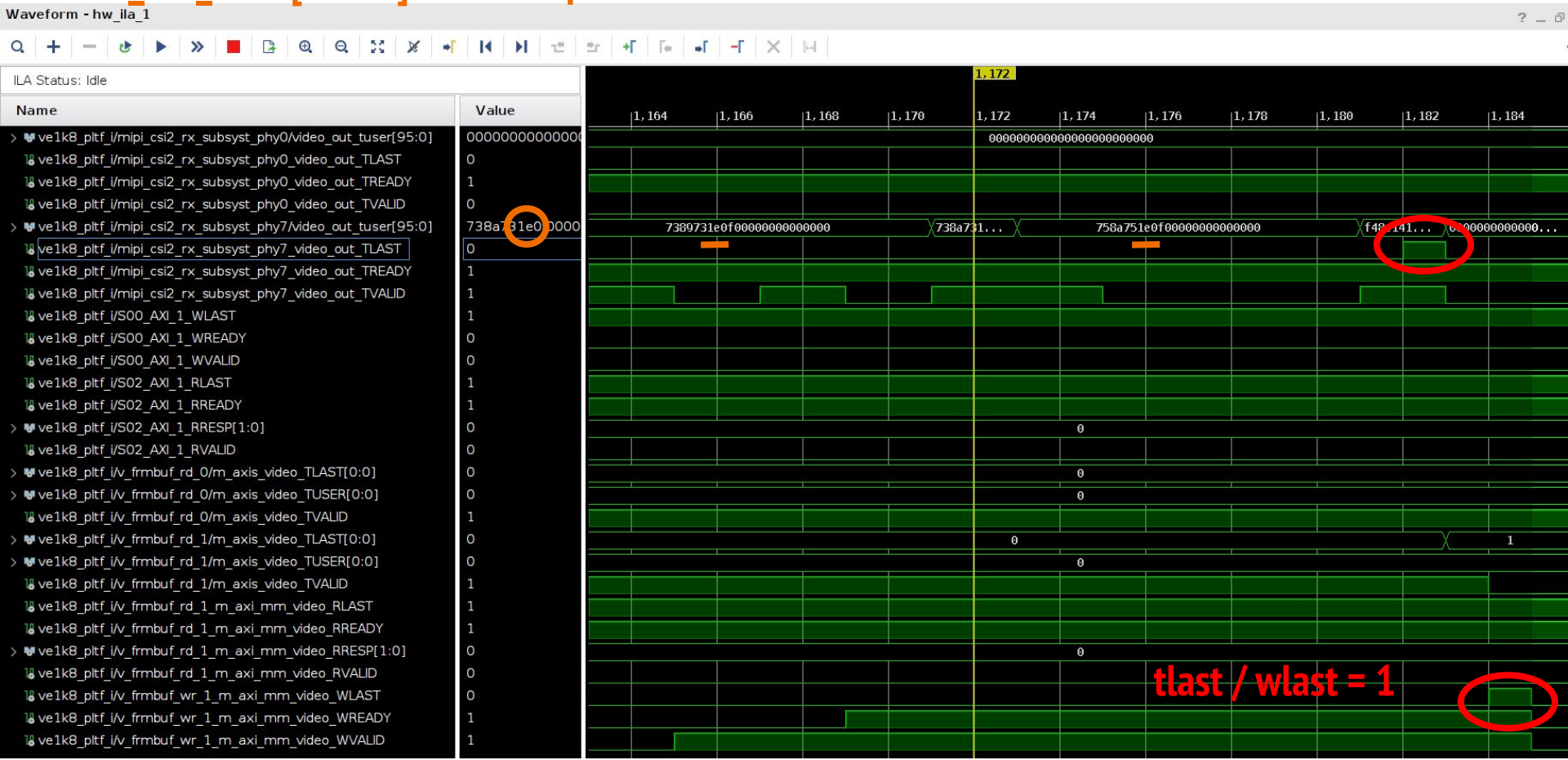
Aug. 20, 2025


Waveform - hw_ila_1
ILA Status: Idle
Name
Value
ve1k8_pltf_i/mipi_csi2_rx_subsyst_phy0/video_out_tuser[95:0]
1886141e0f0000
ve1k8_pltf_i/mipi_csi2_rx_subsyst_phy0_video_out_TLAST
0
ve1k8_pltf_i/mipi_csi2_rx_subsyst_phy0_video_out_TREADY
1
ve1k8_pltf_i/mipi_csi2_rx_subsyst_phy0_video_out_TVALID
0
ve1k8_pltf_i/mipi_csi2_rx_subsyst_phy7/video_out_tuser[95:0]
ve1k8_pltf_i/mipi_csi2_rx_subsyst_phy7_video_out_TLAST
0
ve1k8_pltf_i/mipi_csi2_rx_subsyst_phy7_video_out_TREADY
1
ve1k8_pltf_i/mipi_csi2_rx_subsyst_phy7_video_out_TVALID
0
ve1k8_pltf_i/S00_AXI_1_WLAST
0
ve1k8_pltf_i/S00_AXI_1_WREADY
0
ve1k8_pltf_i/S00_AXI_1_WVALID
0
ve1k8_pltf_i/S02_AXI_1_RLAST
1
ve1k8_pltf_i/S02_AXI_1_RREADY
1
ve1k8_pltf_i/S02_AXI_1_RRESP[1:0]
0
ve1k8_pltf_i/S02_AXI_1_RVALID
0
ve1k8_pltf_i/v_frmbuf_rd_0/m_axis_video_TLAST[0:0]
0
ve1k8_pltf_i/v_frmbuf_rd_0/m_axis_video_TUSER[0:0]
0
ve1k8_pltf_i/v_frmbuf_rd_0/m_axis_video_TVALID
1
ve1k8_pltf_i/v_frmbuf_rd_1/m_axis_video_TLAST[0:0]
0
ve1k8_pltf_i/v_frmbuf_rd_1/m_axis_video_TUSER[0:0]
0
ve1k8_pltf_i/v_frmbuf_rd_1/m_axis_video_TVALID
1
ve1k8_pltf_i/v_frmbuf_rd_1_m_axi_mm_video_RLAST
1
ve1k8_pltf_i/v_frmbuf_rd_1_m_axi_mm_video_RREADY
1
ve1k8_pltf_i/v_frmbuf_rd_1_m_axi_mm_video_RRESP[1:0]
0
ve1k8_pltf_i/v_frmbuf_rd_1_m_axi_mm_video_RVALID
0
ve1k8_pltf_i/v_frmbuf_wr_1_m_axi_mm_video_WLAST
1
ve1k8_pltf_i/v_frmbuf_wr_1_m_axi_mm_video_WREADY
0
ve1k8_pltf_i/v_frmbuf_wr_1_m_axi_mm_video_WVALID
0
1,875
0
500
1,000
1,500
2,000
2,500
3,000
3,500

Both cameras show valid data observed in tuser!

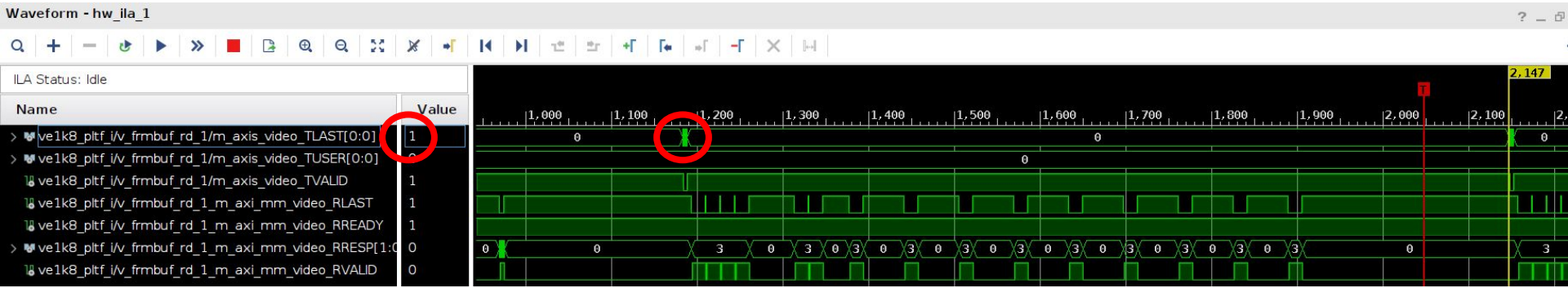


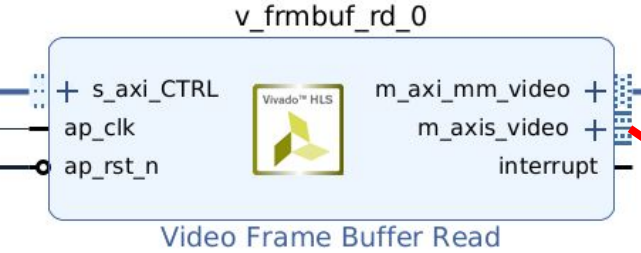
video_out_tuser[69:64] = 0x1e represents YUV422 8-bit



Maybe we can take advantage of tlast data.

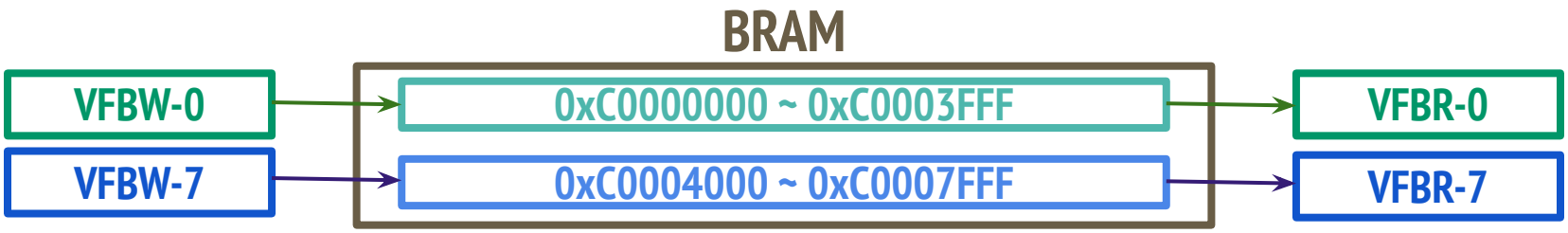
By probing video frame buffer read (VFBR), we can see …





axi_mm is connected to **AXI Interconnect** for **BRAM**

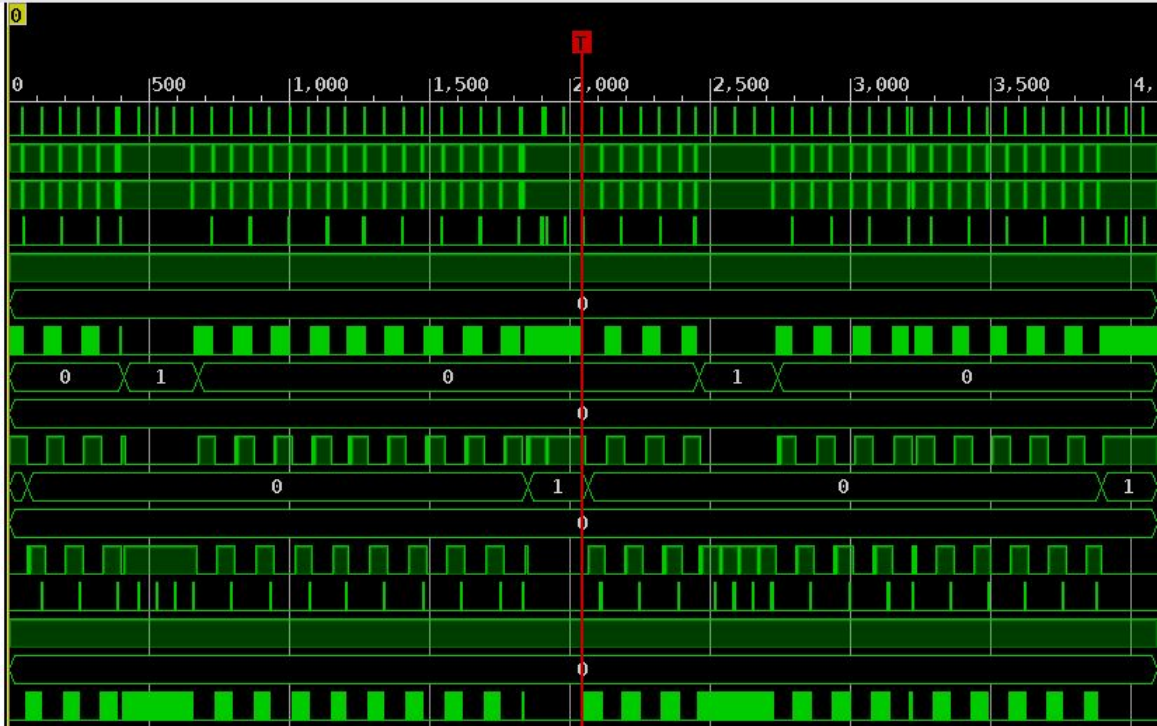
The output axis includes **tlast**.

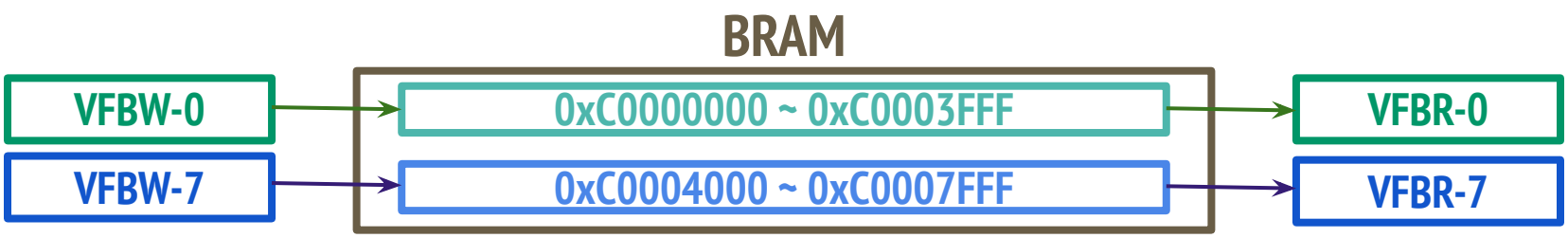


Waveform - hw_ila_1

ILA Status: Idle

Name	Value
ve1k8_pltf_i/axi_interconnect_0_M00_AXI_RLAST	0
ve1k8_pltf_i/axi_interconnect_0_M00_AXI_RREADY	1
ve1k8_pltf_i/axi_interconnect_0_M00_AXI_RVALID	1
ve1k8_pltf_i/S02_AXI_1_RLAST	0
ve1k8_pltf_i/S02_AXI_1_RREADY	1
ve1k8_pltf_i/S02_AXI_1_RRESP[1:0]	0
ve1k8_pltf_i/S02_AXI_1_RVALID	0
ve1k8_pltf_i/v_frmbuf_rd_0/m_axis_video_TLAST[0:0]	0
ve1k8_pltf_i/v_frmbuf_rd_0/m_axis_video_TUSER[0:0]	0
ve1k8_pltf_i/v_frmbuf_rd_0/m_axis_video_TVALID	1
ve1k8_pltf_i/v_frmbuf_rd_1/m_axis_video_TLAST[0:0]	1
ve1k8_pltf_i/v_frmbuf_rd_1/m_axis_video_TUSER[0:0]	0
ve1k8_pltf_i/v_frmbuf_rd_1/m_axis_video_TVALID	0
ve1k8_pltf_i/v_frmbuf_rd_1_m_axi_mm_video_RLAST	0
ve1k8_pltf_i/v_frmbuf_rd_1_m_axi_mm_video_RREADY	1
ve1k8_pltf_i/v_frmbuf_rd..._axi_mm_video_RRESP[1:0]	0
ve1k8_pltf_i/v_frmbuf_rd_1_m_axi_mm_video_RVALID	0





Waveform - hw_ila_1

ILA Status: Idle

Name	Value
ve1k8_pltf_i/axi_interconnect_0_M00_AXI_RLAST	0
ve1k8_pltf_i/axi_interconnect_0_M00_AXI_RREADY	1
ve1k8_pltf_i/axi_interconnect_0_M00_AXI_RVALID	1
ve1k8_pltf_i/v_frmbuf_rd_0/m_axi_video_TLAST[0:0]	0
ve1k8_pltf_i/v_frmbuf_rd_0/m_axi_video_TUSER[0:0]	0
ve1k8_pltf_i/v_frmbuf_rd_0/m_axi_video_TVALID	1
ve1k8_pltf_i/v_frmbuf_rd_1/m_axi_video_TUSER[0:0]	0
ve1k8_pltf_i/v_frmbuf_rd_1/m_axi_video_TVALID	0
ve1k8_pltf_i/v_frmbuf_rd_1_m_axi_mm_video_RREADY	1
ve1k8_pltf_i/v_frmbuf_rd_1_m_axi_mm_video_RVALID	0

BRAM

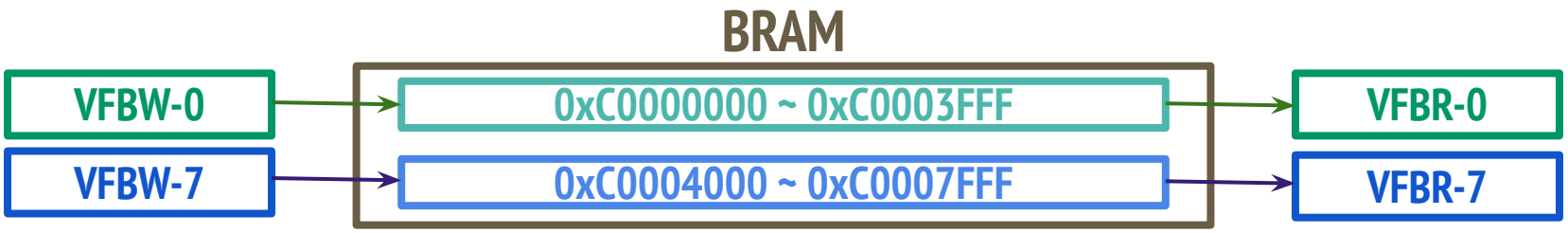
VFBR-0 axi-mm

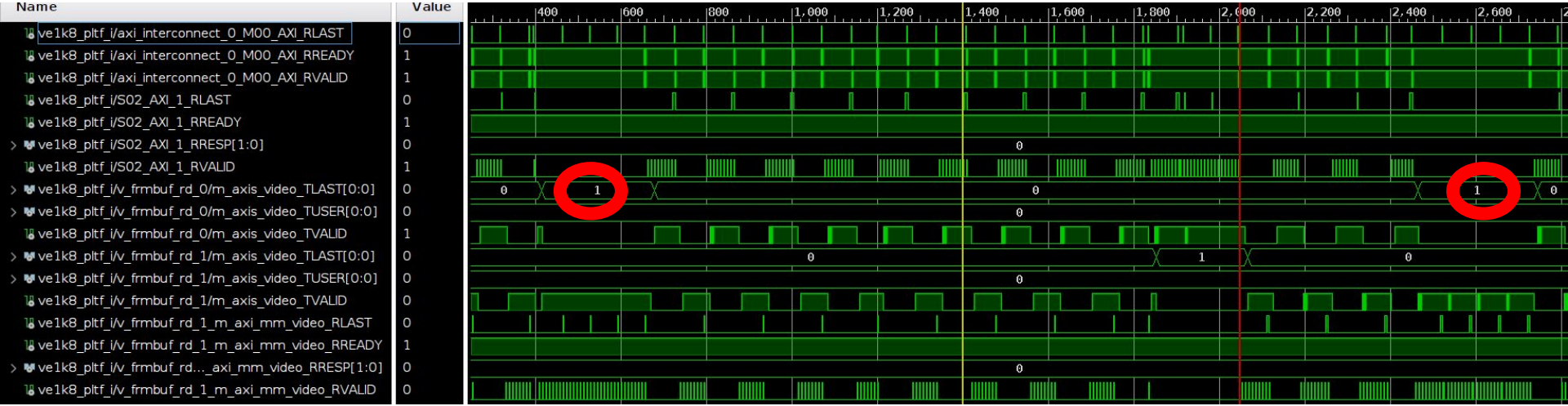
VFBR-0 axis

VFBR-7 axis

VFBR-7 axi-mm

001001001… → regular





David's Comment:

The VFBR reads data in BRAM with a regular pattern (001001001001…)

→ BRAM doesn't know what memory range will store a complete image frame.

→ But both VFBW and VFBR know! → This is why VFBR knows which data is the last.